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PIPELINED MULTIPLEXER BASED FULL ADDER USING CMOS LOGIC

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Abstract-

The efficiency of a system mainly depends on the performance of the internal components present in the system. So, the internal components must be designed in such a way that they should consume less power with increase in speed. Full adder is one of the major components in the design of many sophisticated hardware circuits. Perhaps it is one of the essential components in the design of a wide variety of processors also. In this paper several pipelined multiplexer based CMOS full adder topologies are presented. The main idea is to introduce the design of high performance and low power multiplexer Based cmos transistor full adder which acquires less power and high speed. Due to pipelining we acquire high speed and low power consumption.

Keywords-

full adder,pipelining,power,speed,CMOS**.**

I.INTRODUCTION

Full adder is one of the basic building blocks of many of the digital VLSI circuits. Several refinements has been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation. One of the major advantages in reducing the number of transistors is to put more devices on a single silicon chip there by reducing the total area. In the recent days the use of portable electronic devices like cellular devices, laptops has been

increased exponentially. The main requirement of these portable devices is reduced power consumption, small area and high speed of operation. To achieve these requirements research efforts in the field of low power VLSI (very large scale integration) have increased many folds. As the number of transistors on a single silicon chip increases, the package density also increases. With the rise in chip density, power consumption of VLSI systems is also increasing and this further, adds to reliability and packaging problems. Packaging and cooling cost of VLSI systems also goes up with high power dissipation. So, the low power consumption along with minimum delay and area requirements is one of important design consideration for IC designers in designing portable electronic devices and many sophisticated hardware circuits.

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires requires AND and OR gates.

The basic equations for sum and carry of a full adder are

Sum = A(xor)B(xor)C (1)

Carry = AB + BC + CA (2)

The basic logic diagram for full adder using its Boolean equations with basic gates can be represented as shown below

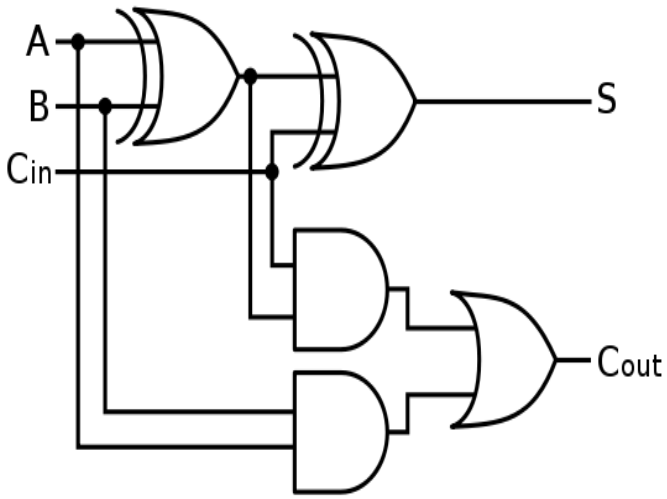

Figure 1: Logic circuit for Full Adder

The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. Several refinements has been made in its structure in terms of transistors to increase the performance of full adder. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip thereby reducing the area and delay. In the proposed work the XOR gate is implemented with only two transistors which reduces the area to a large extent and power consumption.

The full adder design in static CMOS using complementary pull up pMOS network and pull down nMOS network is the most conventional

one, and it also has the advantage of very low power consumption. However, it has as many as 28transistors and thus requires considerable chip area for its implementation. The full adder design based on CMOS transmission gates and CMOS inverters uses 20 transistors. The circuit can operate with full output voltage swing. The designs were further reduced to only 16 transistors while maintaining the full output voltage swing operation. To further minimize the number of transistors, pass transistor logic can be used in lieu of transmission gate. Pass transistor logic based XOR and XNOR circuits were used and as a result the full adder design consists of only 14transistors. In this design, an inverter is employed to generate the function AΘB. The full adder can be implemented in terms of two half adders. It can be represented in the form of modules as

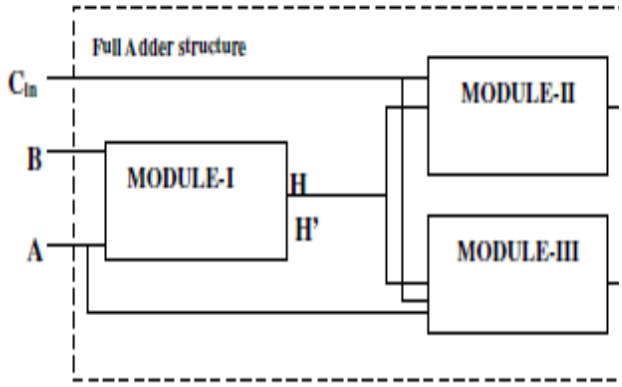

Figure 2:structure of full adder.

II.ESISTING FULLADDER USING PASS TRANSISTOR LOGIC

In the present paper the full adder is implemented by using multipler based pass transistor logic that uses MOSFETs as its basic components. Further the logic is implemented seperately for pmos transistors, nmos transistors and cmos transistors. The same happens when a PMOS transistor is being considered. In this case the 0 input logic value when transmitted is not totally propagated, and a Vth voltage remains stored in the output capacitance. The same happens when a PMOS transistor is being considered. In this case the 0 input logic value when transmitted is not totally propagated, and a Vth voltage remains stored in the output capacitance.

In the present paper, the logic for multiplexer is realized using pass transistor logic. The number of transistor count can be decreased by implementing pass transistor logic in the multiplexers. Further, the pass transistor logic is implemented in multiplexer for pmos, nmos and cmos transistors separately.

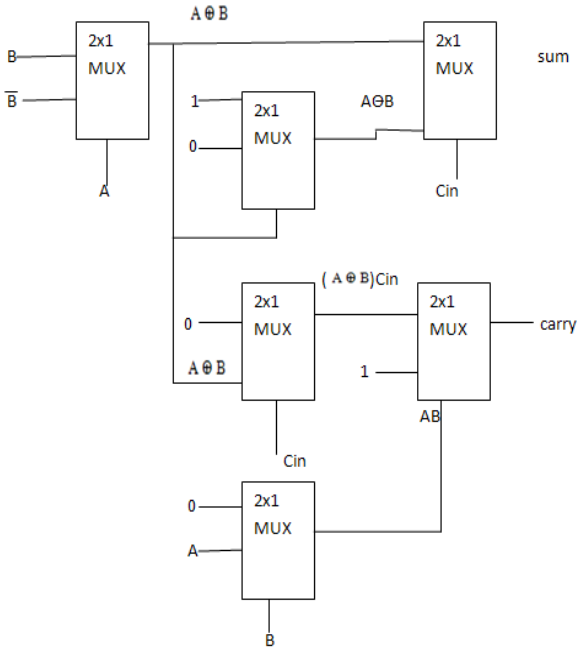

Figure 3:Multiplexer based full adder using Pass transistor logic

Pass transistor logic is used to improve the performance of arithmetic and logic circuits. This logic can be used to reduce the power dissipation in the system and to increase the speed of operation of the processor. By using pass transistor logic the number of transistor count can also be reduced when compared to static CMOS design in realizing th complex systems. When the number of transistor are decreased the area of the chip decreases in parallel.When the number of transistors is reduced, we can decrease the number of layout elements and parasitic capacitances. Several parasitic capacitances are charging and discharging during signal propagation, and some current is consumed. Therefore, PTL design can

be used to remove some transistors, and, it may be important to reduce the current consumption. However, some electrical problems must be addressed. There are situations in which the input signal of a PTL gate is passed to the output node, but the output signal sometimes can be degraded. For instance, the 1 input logic value when transmitted through a NMOS transistor cannot charge the output parasitic capacitance to Vdd level. The maximum voltage stored by the output capacitance is Vdd-Vth. Vth is the threshold voltage of theNMOS transistor.

The figure 3 shows the block diagram for the design of full adder using multiplexers that uses pass transistor logic as its basic building logic. The logic is implemented using six 2x1 multiplexers which has two inputs and one output for each multiplexer with a selecet line in its structure. The output is generated depending on the selection line only. These multiplexers can be designed with the help of pass transistor logic that uses both PMOS and NMOS transistors.

III.PROPOSED PIPELINED MULTIPLEXER BASED FULLADDER USING CMOS TRANSISTOR LOGIC

As we want to reduce the power consumption increase the speed, accuracy of the system we go for pipelining concept. Here we are modifying the existing work by pipelining the full adder multiplexer. In the modified pipelined concept we are using cmos logic Hence we obtain good speed and low power consumption is obtained.

D FLIP FLOP

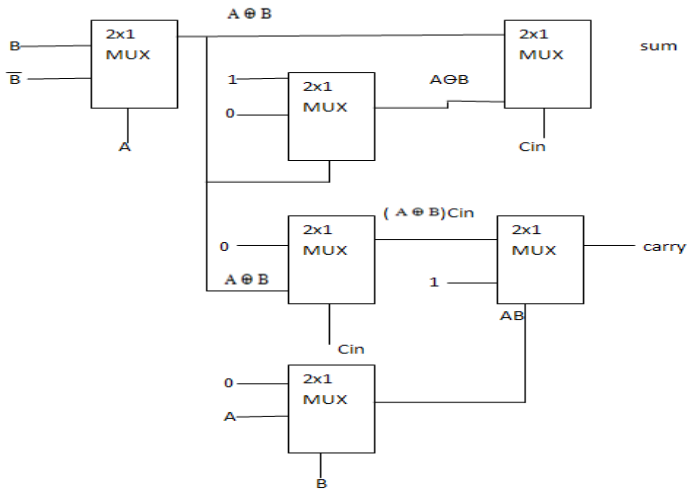

Figure 4:pipelined multiplexer fulladder

IV.SIMULATION RESULTS

The simulation results for the proposed logic are

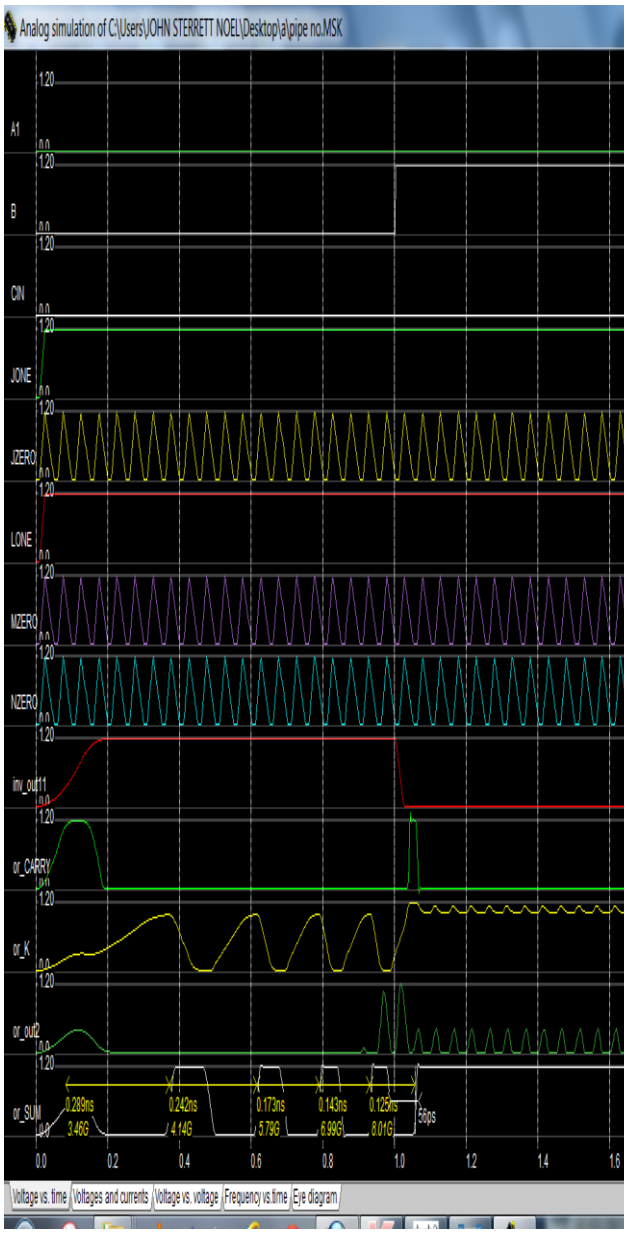

Figure 5: Simulation result of multiplexer based full adder using Cmos logic without pipelining

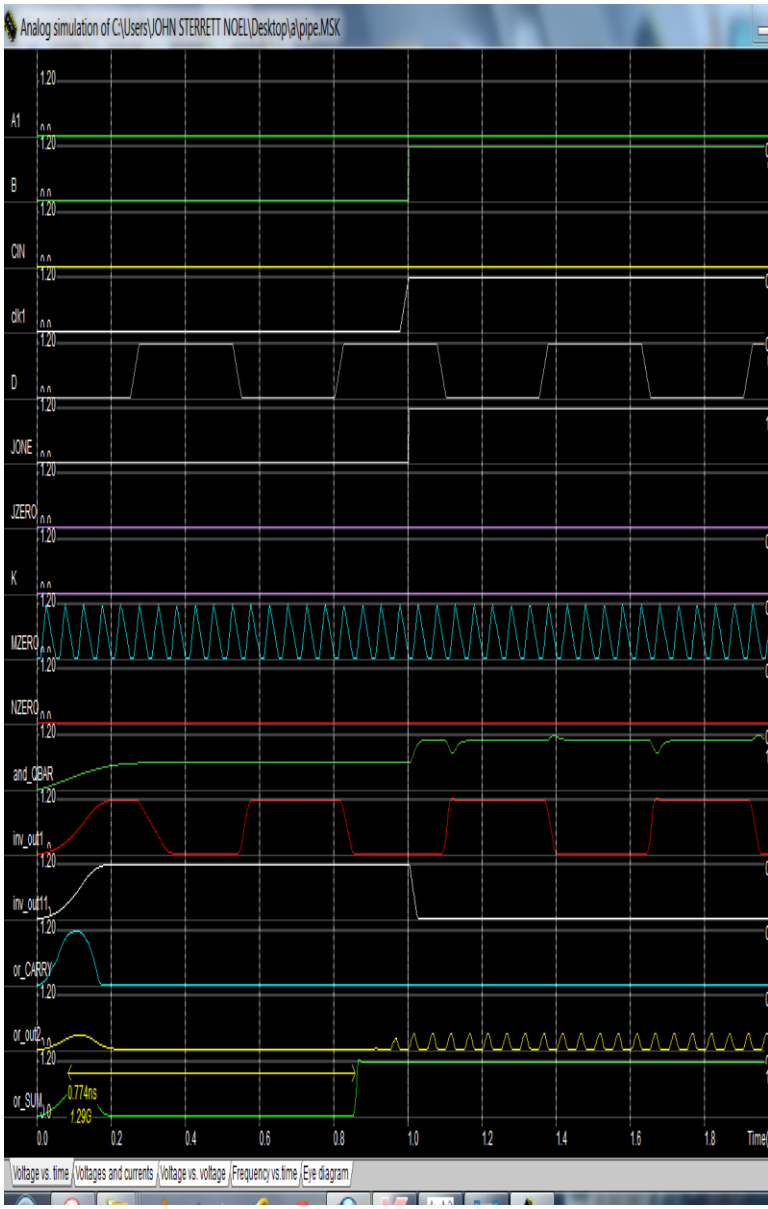

Figure 6:Simulation result of pipelined multiplexer based full adder using Cmos logic

Table 1.Performance perameters of proposed full adders

Performance parameters of proposed full adders

parameter	Power consumed(watts)	Number of transistors
Mixed CMOS	393.9778P	14
Pass transistor Pmos(sum)	3.1933U	10
Pass transistor Pmos(carry)	638.2011N	12
Pass transistor Nmos(sum)	9.0434P	10
Pass transistor Nmos(carry)	9.0434P	12
CMOS full adder	0.631mw	84
CMOS pipelined full adder	0.591mw	116

From table 1, it can be observed that the power dissipation of pipelined CMOS full adder is less comared to CMOS full adder without pipeline adder circuits. Because of these advantages it can be used in many of the low power applications which is considered to be an important feature in portable devices.

V.CONCLUSION

In the present work, the full adder design is realized in three different ways with the help of PMOS, NMOS and CMOS transistors and pipelining concept is introduced as to reduce power Consumption and to obtain speed, accuracy.here the pipelining concept is introduced in CMOS and pass transistor logic in multiplexer based full adder and hence the power analysis parameters are compared. Simulation result shows that this proposed full adder achieves better power reduction when compared with other commonly used full adders.

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